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SF-6541

B. E. - II (Sem. - IV) (IT) Examination

May/June – 2011

Electronics - II

(Old Course)

Time : Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ B. E. - 2 (SEM. - 4) (IT)

Name of the Subject :

☛ ELECTRONICS - 2 (OLD COURSE)

☛ Subject Code No. : 6 5 4 1 ☛ Section No. (1, 2,.....) : Nil.

Seat No. :

Student's Signature

(2) Attempt **all** questions.
(3) Figures to the **right** hand side indicates full marks.
(4) Make assumption wherever is necessary.

1 (a) Attempt the following : **10**

(i) Transfer function for voltage series negative feedback amplifier is_____

(ii) Desensitivity D for current series negative feedback amplifier is _____.

(iii) The relationship between gain with feedback and gain without feedback is given by _____ for negative amplifier.

(iv) The efficiency of inductor coupled class of amplifier is _____.

(v) Distortion with negative feedback _____.

(vi) 7912 IC gives us _____as output voltage.

(vii) Input impedance of current shunt amplifier with feedback _____.

(viii) Figure of merit is defined as _____.

(ix) 78XX ICs removes ripule also. True/False. Justify.

(x) The feedback factor β for the transconductance is _____.

(b) Explain by load line and power calculation how inductor coupled class of power amplifier increases maximum efficiency to 50%. **5**

(c) The transistor used in inductor coupled amplifier has rating Pc_{max} = 16 W. BV_{CEO} = 60V, Ic_{max} = 4A. Determine the maximum attainable swing and power dissipated to load. Assume VCESAT = 0V and load resistance RL = 8 Ω. **5**

2 Attempt any **two** of the following : **15**

(a) Explain the basic block diagram of feedback amplifier. Enlist the steps to recognize the type of topology of given feedback amplifier.

(b) For the circuit shown in figure 1 the transistor parameters are hfe = 50, hie = 1 kΩ find

(i) i_L/i_s

(ii) V_o/V_s

(iii) i_L/V_s

(iv) $_V o_{/i} s$

(v) R_{if}

(vi) R_{of}

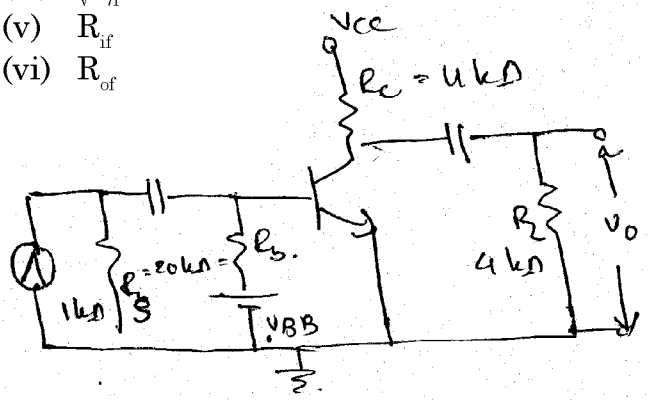

Fig.1

(c) An amplifier with open loop voltage gain Av = 1000 ± 100 is available. Design the feedback amplifier whose voltage gain varies by no more than ± 0.1%

3 Attempt any three : **15**

(a) State different features of 78 XX series voltage regulators.

(b) Explain different performance measurement of voltage regulators.

(c) Explain design of low voltage using IC 723.

(d) Draw neat and clean diagram of series and shunt voltage regulator. Write drawbacks in both regulators.

4 (a) Do as directed : **10**

(i) Define : Input Offset voltage
Input offset current

(ii) What are the limitations of open loop configurations.

(iii) Define : Load regulation.

(iv) Explain the basic principal of oscillators.

(v) Applications of 555 timer.

(b) Draw and explain the ckt diagram for summing, scaling and averaging amplifier using op-amp. 8

OR

(b) Draw the ckt diagram of Integrator and explain the same. 8

5 (a) Explain Wein bridge oscillator. 8

OR

(a) Explain the first order high pass butterworth filter. 8

(b) Explain the working of monostable multivibrator using op-amp and obtain the expression for the output pulse width and recovery time. 8

6 Attempt any **two** : **16**

(i) Explain the block diagram of basic voltage regulator.

(ii) Bistable multivibrator

(iii) Phase locked loop

(iv) SMPS